



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 09/498,064 | 02/04/2000 | Hirofumi Ihara | N99135G-US | 8280 |
| 21254 | 7590 | 06/10/2003 | | |
| MCGINN & GIBB, PLLC 8321 OLD COURTHOUSE ROAD SUITE 200 VIENNA, VA 22182-3817 | | | EXAMINER | |
| | | | CHUNG, DAVID Y | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2871 | |

DATE MAILED: 06/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | |
|-----------------------------|------------------------|---------------------|
| Offic Action Summary | Application No. | Applicant(s) |
| | 09/498,064 | IHARA, HIROFUMI |
| | Examiner | Art Unit |
| | David Y. Chung | 2871 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 02 April 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-32 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

| | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-32 rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (U.S. 6,184,945) in further view of Yamazaki et al. (U.S. 6,118,506).

As to claims 1-8, 13-22, 31 and 32, Sung discloses a liquid crystal display wherein an electrode film forming a capacitor in cooperation with the pixel electrode is connected to the gate wiring via a connecting path. Note the following elements in figures 4 and 5: source electrode 85, electrode film 103 forming a capacitor with pixel electrode 88, insulating layers 92 and 100, and connecting path 107 for connecting gate line 86 to the electrode film 103. See columns 8 and 9 of the specification. Sung teaches that the source electrodes, source wires, drain electrodes, and capacitive electrodes are patterned from the same conductive metal film using the same mask. See column 10, lines 12 – 30.

Sung does not teach varying the thickness and dielectric material of the two insulating layers in order to control the respective capacitances. Yamazaki discloses a

Art Unit: 2871

liquid crystal display wherein the insulating layer between the gate electrode and auxiliary capacitance electrode is thicker and has a lower dielectric constant than the insulating layer between the auxiliary capacitance electrode and pixel electrode.

Yamazaki teaches that a dielectric film with a minimum dielectric constant and large thickness is used as insulating film 315 between the gate and auxiliary capacitance electrode in order to minimize parasitic capacitance. Yamazaki teaches that a dielectric film having a maximum relative dielectric constant and small thickness is used as insulating film 317 between the auxiliary capacitance electrode and pixel electrode in order to create retaining capacitors having desired capacitance. Yamazaki teaches that the disclosed structure creates retaining capacitors having the minimum necessary capacitance while suppressing parasitic capacitances without sacrificing the aperture ratio. See column 7, lines 22 – 51. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to vary the thickness and dielectric material of the insulating layers in Sung because of the benefits taught by Yamazaki.

As to claim 9, it was well known and obvious to form a multi-layer insulating film in order to improve TFT performance while improving TFT thermal and electrical stability at the same time. Evidence of this is found in the disclosure of Gu et al. (U.S. 6,011,274). Gu discloses an organic layer 33 for reducing cross talk and an inorganic layer 32 for eliminating potential TFT off current and large sub threshold slope. See column 6, lines 48 – 58. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to form a multi-layer upper insulating layer in the

Art Unit: 2871

device of Sung in order to improve TFT performance and TFT reliability at the same time.

As to claim 10, Yamazaki teaches that the upper insulating layer is preferably formed of silicon-oxide based dielectric film because of the large dielectric constants that can be obtained. See column 6, lines 57 – 63. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to form the upper insulating layer in Sung of a silicon-oxide based dielectric film in order to obtain a large dielectric constant and thereby increase the capacitance value of the auxiliary capacitor.

As to claim 11, it was well known and obvious to form auxiliary capacitance common wiring in order to apply a common potential to each of the auxiliary capacitor electrodes. Keeping each of the auxiliary capacitor electrodes at a common voltage, typically ground, allowed stable operation of the display device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to provide auxiliary capacitance common wiring in the device of Sung in order to ensure stable operation.

As to claim 12, it was well known and obvious to create multiple contacts between any two conductive elements in order to improve the electrical connection between them. This would improve the reliability of the device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to provide

Art Unit: 2871

multiple contacts between the auxiliary capacitor electrode and gate wiring or between the auxiliary capacitor electrode and capacitance common wiring in order to ensure the reliability of the display.

As to claim 23, figure 5 of Sung clearly shows gate wire 86 formed directly on insulating substrate 90. Gate insulating film 92 is formed directly on gate wire 86.

As to claims 24-26, 28 and 29, figure 5 of Sung clearly shows source wire 85 and first electrode film 103 formed directly on gate insulating film 92. Second insulating film 100 is formed directly on source wire 85 and first electrode film 103. Pixel electrode 88 is formed directly on second insulating film 100.

As to claim 27, figure 5 of Sung clearly shows the gate wire 86 and the first electrode film 103 being separated by a single layer comprising the gate insulating film 92. The first electrode film 103 and pixel electrode 88 are separated by a single layer comprising second insulating film 100.

As to claim 30, Sung does not disclose a black matrix. However, it was well known and obvious to form a black matrix overlapping both the edges of the pixel and regions between adjacent pixels. It was well known and obvious to do this in order to prevent light leakage and maintain good contrast as well as to shield regions of disclination within the pixels. Therefore, it would have been obvious to one of ordinary

Art Unit: 2871

skill in the art at the time of invention to form a black matrix on the capacitor section in order to prevent light leakage and shield regions of disclination.

Response to Arguments

Applicant's arguments filed April 2, 2003 have been fully considered but they are not persuasive. Sung teaches all of the features of claim 1 except making the upper insulating film 100 having a smaller thickness and higher dielectric constant than the gate insulating film 92. Yamazaki et al. teaches forming a thick insulation with a small dielectric constant between two elements forming a parasitic capacitance and forming a thin insulation with a large dielectric constant between two elements forming a retaining capacitor. In figure 5 of Sung, it would have been obvious to make the upper insulating film 100 having a smaller thickness and higher dielectric constant than the gate insulating film 92 in order to minimize the parasitic capacitance between the gate wire 86 and pixel electrode 88 while maximizing the retaining capacitance formed between pixel electrode 88 and first electrode film 103. Examiner does not see anything in the language of Sung cited by applicant that would constitute a teaching away from making the upper insulating layer 100 having a smaller thickness and larger dielectric constant than gate insulating layer 92.

In response to applicant's argument that the references of Sung and Yamazaki et al. would not have been combined as argued by the examiner, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly

Art Unit: 2871

suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.

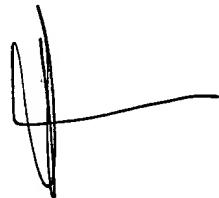
See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Chung whose telephone number is (703) 306-0155. The examiner can normally be reached on Monday-Friday from 8:30 am to 5:00 pm.



KENNETH PARKER
PRIMARY EXAMINER

David Chung
GAU 2871
06/05/03